Claims

1. A method of designing devices in integrated circuits, the method comprising:

translating select device parameters in a first database associated with a first process to device parameters in a second database associated with a second process; and

displaying a design based on the device parameters in the second database.

2. The method of claim 1, wherein the select device parameters are at least one of schematic and layout parameters.

3. The method of claim 1, wherein the select device parameters are schematic parameters, the schematic parameters including resistances, the method further comprising:

retaining select resistance parameters of the first database in the second database.

4. The method of claim 1, wherein the select device parameters are schematic parameters, the schematic parameters including capacitances, the method further comprising:

retaining select capacitance parameters of the first database in the second database.

5. The method of claim 1, wherein the select device parameters are layout parameters, the layout parameters including device geometry parameters, the method further comprising:

retaining select geometry parameters of the first database in the second database.

6. The method of claim 1, wherein the design displayed is a schematic design.

7. The method of claim 1, wherein the design displayed is a layout display.

8. The method of claim 1, wherein translating select device parameters further comprises:

mapping mask layers.

9. The method of claim 1, wherein translating select device parameters further comprises:

selectively adding extra interconnect layers.

10. The method of claim 1, wherein translating select device parameters further comprises:

preserving instance names between the first and second databases.

11. The method of claim 1, wherein translating select device parameters further comprises:

checking and correcting grid and line mode automatically.

12. The method of claim 1, further comprising:

displaying an original design based on the device parameters in the first database along side the design based on the translated device parameters in the second database.

13. The method of claim 12, wherein a separate design session is not required to display the original design based on the parameters in the first database.

14. A method of translating an integrated circuit design in a first process to a second process, the method comprising:

setting translations options;

reading original schematic information;

translating schematic information;

reading original layout information;

translating layout information; and

outputting parameters of translated schematic and layout information.

15. The method of claim 14, further comprising:

copying a source library to a new process library.

16. The method of claim 14, further comprising:

selecting a target library, wherein the target library contains information translated to the second process.

17. The method of claim 14, further comprising:

writing original schematic information into a new data base.

18. The method of claim 14, further comprising:

adding and deleting wires automatically to keep electrically correct schematic designs.

19. The method of claim 14, further comprising:

writing original layout information into a new database.

20. The method of claim 14, further comprising:

mapping mask layers.

21. The method of claim 14, further comprising:

selectively adding extra interconnect layers.

22. The method of claim 14, further comprising:

checking and correcting grid and line mode automatically.

23. The method of claim 14, further comprising:

restoring conductivity in a translated layout from schematic information.

24. The method of claim 14, further comprising:

preserving interconnect lines.

25. The method of claim 14, further comprising:

generating a report when a limitation is encountered during a translation process.

26. The method of claim 14, further comprising:

creating a configuration file; and

reading the configuration file.

27. The method of claim 26, wherein creating a configuration file further comprises at least one of the functions in the group of functions comprising, mapping devices, mapping terminals, mapping mask layers, mapping parameters, inserting original device parameters, creating polarity and rotation, defining resistor and capacitor options, defining interconnect options and defining functions to be triggered after translation.

28. The method of claim 14, further comprising:

displaying a translated schematic design.

29. The method of claim 28, further comprising:

displaying an original schematic design based on the original schematic information along side the translated schematic design.

30. The method of claim 14, further comprising:

displaying a translated layout design.

31. The method of claim 30, further comprising:

displaying an original layout design based on the original layout information along side the translated layout design.

32. The method of claim 14, wherein setting translation options further comprises at least one of an option from a group of options comprising, setting select resistances to remain unchanged, setting select capacitances to remain unchanged, setting select geometries to remain unchanged and a layout interconnect option.

33. The method of claim 32, wherein setting translation options is done with the use of a graphic user interface.

34. The method of claim 14, further comprising:

displaying the outputted parameters of the translated schematic and layout information.

35. The method of claim 34, further comprising:

displaying original parameters associated with the original schematic and layout information along side the outputted parameters.

36. The method of claim 35, wherein the side by side display is created without having to start a separate design session.

37. A computer-readable medium including instructions for simulating the design of an integrated circuit from one process to another process comprising:

processing translation options;

reading original schematic information;

translating schematic information;

reading original layout information;

translating layout information; and

outputting parameters of translated schematic and layout information.

38. The computer-readable medium of claim 37, further comprising:

copying a source library to a new process library.

39. The computer-readable medium of claim 37, further comprising:

selecting a target library, wherein the target library contains information translated to the second process.

40. The computer-readable medium of claim 37, further comprising:

writing original schematic information into a new data base.

41. The computer-readable medium of claim 37, further comprising:

adding and deleting wires to keep electrically correct schematic designs.

42. The computer-readable medium of claim 37, further comprising:

writing original layout information into a new database.

43. The computer-readable medium of claim 37, further comprising:

mapping mask layers.

44. The computer-readable medium of claim 37, further comprising:

selectively adding extra interconnect layers.

45. The computer-readable medium of claim 37, further comprising:

checking and correcting grid and line mode automatically.

46. The computer-readable medium of claim 37, further comprising:
restoring conductivity in a translated layout from schematic information.

47. The computer-readable medium of claim 37, further comprising:
preserving interconnect lines.

48. The computer-readable medium of claim 37, further comprising:
generating a report when a limitation is encountered during a translation process.

49. The computer-readable medium of claim 37, further comprising:
displaying the outputted parameters of the translated schematic and layout information.

50. The computer-readable medium of claim 37, wherein setting translation options further comprises at least one of an option from a group of options comprising, setting select resistances to remain unchanged, setting select capacitances to remain unchanged, setting select geometries to remain unchanged and a layout interconnect option.